**Methods of estimation and reduction of switching activity of VLSI circuit**

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**Acknowledgement**

We would like to convey my heartfelt gratitude to **SUBRATA DAS** for his tremendous support and assistance in the completion of my project. I would also like to thank our **HOD, PROF. Anirban Mitra**, for providing me with this wonderful opportunity to work on a project with the topic Methods of estimation and reduction of switching activity of VLSI circuit. The completion of the project would not have been possible without their help and insights.

07/02/2023

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**Content Page No**

1. **Introduction**
2. **Methodology**
   1. **Problem Specification**
   2. **Significance of the proposed problem**
3. **Literature Review**
4. **Detailed Methodology**
5. **Conclusions and Future Plan**

**Acknowledgement**

**References**

1. **INTRODUCTION:**

**Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device.**

**Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.**

Traditionally, the major concerns of VLSI designers include minimization of the chip area, enhancement of performance, testability, and reduction of manufacturing cost and the improvement of reliability. With increasing use of portable devices and wireless communication systems, the reduction of energy consumption and hence the reduction of power dissipation and optimization of chip temperature are current issues in recent VLSI design. In this project we are trying to make a computer programme and a web based application which will use the Algorithm Minimize Switching Activity in The paper “A Rule-Based Approach for Minimizing Power Dissipation of Digital Circuits”.

# METHODOLOGY:

* 1. **PROBLEM SPECIFICATION**

Aggressive device scaling also causes excessive increase in power per unit area of the chip. As such, heat generation and its removal from a chip is a matter of serious concern in 𝐶𝑀𝑂𝑆 circuits the three primary sources of power dissipation are:

* + - The switching activity occurs due to logic transitions. When the nodes of a digital circuit make transition back and forth between two logic levels, parasitic capacitances are charged and discharged. Consequently current flows through the channel resistance of the transistors, and electrical energy is converted into heat
    - The short-circuit current that flows from supply to ground when both the 𝑝-subnetwork and 𝑛-subnetwork of a 𝐶𝑀𝑂𝑆 gate conduct.
    - The leakage current caused by substrate injection at 𝑝-𝑛 junctions and sub-threshold effects determined by the fabrication technology.

To properly mitigate the heat generated by the VLSI chip, there needs to be a proper way to estimate/calculate it.

# WHY IS THIS PROBLEM SIGNIFICANT / NEED FOR THE STUDY

The first two sources of power dissipation are known as dynamic power dissipation and the third one constitutes the static power dissipation. In the present-day technology about 80% of the total power loss occurs due to the switching activity. Thus, minimization of the power dissipation of VLSI circuits necessitates minimization of the dynamic power and hence minimization of the switching activity. Minimization of switching activity can be done at the logic optimization stage. However, the focus of earlier logic optimisation works is primarily on reducing the number of appearances of literals, minimum number of literals in a Sum of Products (SOP) or Product of Sums (POS) expression and the minimum number of terms in an SOP expression.

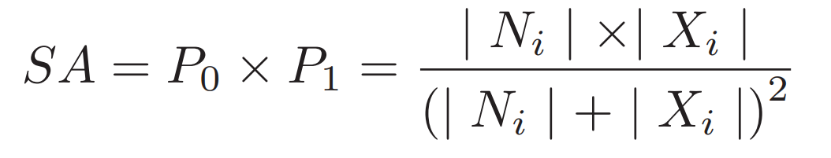
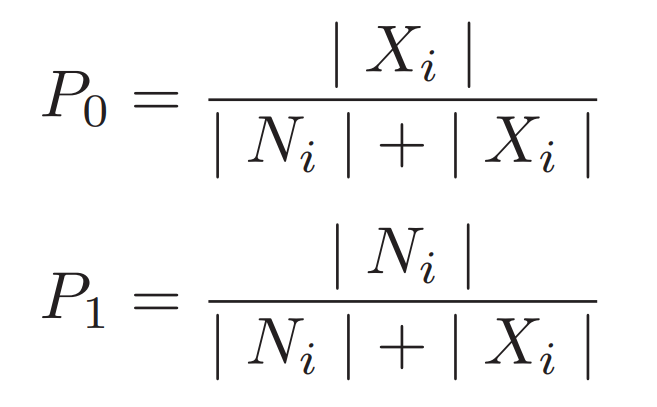
Power consumption can typically be calculated for a single gate in a logic circuit, either by hand or with simulation tools. When many logic circuits switch during operation, it can be challenging to calculate the power consumption directly. If the power consumption can be dependably estimated, this number can be used in thermal simulations to assess reliability and determine appropriate packaging.

1. **LITERATURE REVIEW / RELATED RESEARCH OUTCOMES**

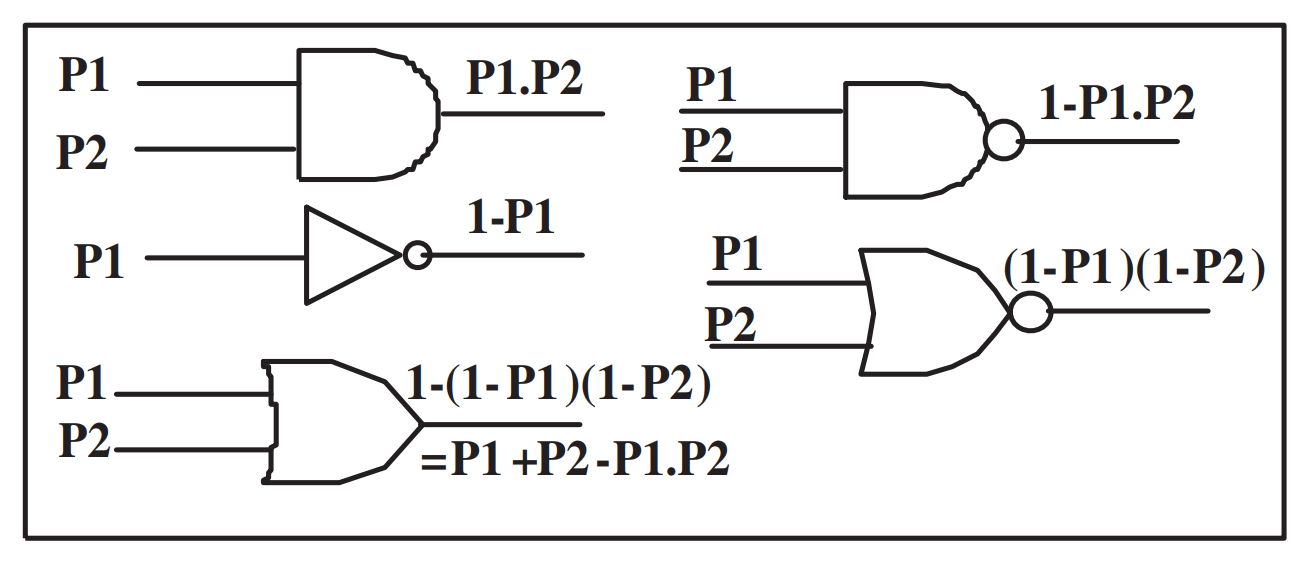
Minimization of power consumption of CMOS digital circuits is studied in the past, considering all levels of the design such as physical, circuit and logic level.In digital CMOS circuits the measure of power dissipation is the circuit switching activity or the average number of transitions. Minimization of the average number of transitions of CMOS digital circuits nodes is discussed in [6]. The work in [7] provides an interesting repository of recent techniques of power modeling and low-power design based on high-level synthesis. The evaluation and the reduction of the switching activity in combinational logic circuits considering both the transitions 1 → 0 and 0 → 1 at any output node is proposed in . In order to satisfy the classical probabilistic approach that limits the maximum value of the switching activity to 1, the definition of the switching activity as proposed in “Minimization of Power Consumption in Digital Integrated Circuits of Reduction of Switching Activity” was customized in [1]. An algorithmic approach at the gate level using Karnaugh maps for reducing the switching activity in combinational logic circuits is presented in [2]. However, the use of Karnaugh maps restricts the number of variables to around 6. Moreover, for the method proposed in [2], the switching activity can be minimized only for some specific switching functions. In [3] the authors proposed a method to estimate the switching activity using a variable delay model. The work of [4] has discussed the system level dynamic power management in chip multiprocessor (CMP) architectures. [5] proposed an algorithm to minimize logic functions with reduced area and interconnects that will improve the circuit performance. Pre-computation-based optimization for low power that computes the output logic values of the circuit in one clock cycle before they are computed, was discussed in [16].

1. **DETAIL METHODOLOGY**

In here the P1 and P2 is the probability of the inputs. Then we calculate the resultant switching activity For a logic expression of a switching function for an output node 𝑖, let ∣ 𝑁𝑖 ∣ and ∣ 𝑋𝑖 ∣ represent the number of 1’s and the number of 0’s. The probabilities of occurrence of a 0 and a 1 respectively at the output node 𝑖 are given by the following equations:

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To calculate the switching activity of a logic circuit, it is important to determine the switching activity for the constituent logic gates. Based on the classical probabilistic definition of the switching activity [11], we can easily calculate the switching activity of the basic gates. For a 𝐴𝑁𝐷, 𝑂𝑅, 𝑁𝐴𝑁𝐷 and 𝑁𝑂𝑅 gate with 𝑛 inputs, the output is 0 or 1 for exactly one input combination (input vector). Hence the value of ∣ 𝑁𝑖 ∣ or ∣ 𝑋𝑖 ∣ is 1 or 2𝑛 − 1. Hence 𝑃0 = 1/2𝑛 or 2𝑛−1/2𝑛, respectively, and the corresponding 𝑃1 = 2𝑛−1/2𝑛 or 1/2𝑛. Thus, the switching activity is given by 2𝑛−1/22𝑛. Hence, as the number of inputs to the above mentioned logic gates increases, the switching activity of these gates decreases. It is clear to see that the switching activity for the 𝑁𝑂𝑇 gate is maximum and of value 1/4 . The switching activity for 𝑋𝑂𝑅 and 𝑋𝑁𝑂𝑅 gates is independent of the number of inputs to the gate and is equal to 1/4 .

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The controllability/observability concepts as described in [19] can also be used to calculate the switching activity. Unfortunately, both approaches give inaccurate results in presence of reconvergent paths. The approach presented in [20] tries to partially solve this problem.

As we have done comparison between The Switching Activity through the Truth Table method and The Probability method that was mentioned here, it was found that there is a variation of difference in relation to how the Boolean expression is denoted.

Lets take a look at “A.B+B.C+C.A” expression ,

The truth table for this expression is

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | AB | BC | CA | AB+BC | AB+BC+CA |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1. **Conclusions and Future plan**

As seen in the data representation it can be seen that our method have given the switching activity given within 20% of error than the truth table method. But the truth table method have taken much more time and work to get the overall switching activity than our proposed method. As such we only taken 3 input variable expressions for this project or it would have been complex to get the truth tables of expressions with more than 3 inputs.

For our next step would be to minimize the difference/error in our method and the truth table switching activity estimation, then propose an Algorithm to reduce the switching activity which help reduce the overall heat output.

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